



The Evolution of DDR

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Agenda

- A little history/future of DRAM (DDR)
- What drives memory market transition?
- Traditional system requirements
- What is different about DDR3?
- Forecast of the market

Disclaimer about DDR3

The DDR3 material in this presentation is a work in progress. DDR3 is not finished with the balloting process nor is it approved as a final JEDEC standard. Some modifications and/or additions will likely take place before final approval. Users should not rely on this presentation as indicative of the content of the final DDR3 standard. JEDEC does not endorse the content of this presentation. The views expressed are solely those of the author(s).

Industry Standard DRAM Evolution

PM → FPM → EDO → SDRAM → DDR → DDR2 → DDR3

-Simple
RAS/CAS

-Fast
CAS
Access

-Latched
Output

-Synchronous
w/Clock
-Multi-Bank
-Programmable
Burst &
Latency
-LVTTL
Interface

-Data
Read/Write
on Both
CLK Edges
-Data Strobe
-SSTL 2.5
Interface

-ODT
-OCD
-Posted CAS
-SSTL 1.8
Interface

Faster
Lower Power

- The Industry Practically Requires an Evolutionary Path
- Every Generation of DRAM adds 3 to 5 features to keep up with system demands without really disturbing the other thousand things that make up a DRAM
- Foundry technology improves some things as well as forcing ever lower core voltage

Transitions to New Technology

- User must see a benefit before widespread adoption takes place
 - Typically the same frequency is not sufficient - 2 speed grades becomes compelling (DDR1-400 => DDR2-667)
- Infrastructure must be in place
 - Multiple suppliers are in volume production
 - Quality chipsets/systems are available

AND of Course =>

Industry DRAM Philosophy

- The Most Important Parameter

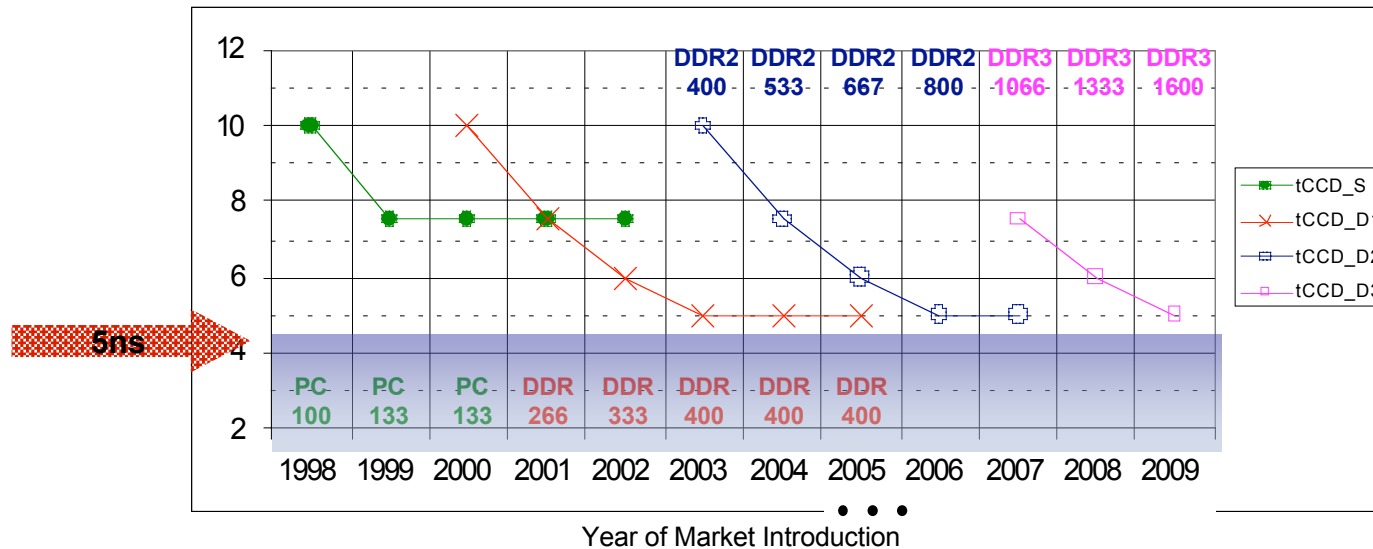
“Price”

- The end user reminds us every day
- The industry maintains low cost by:
 - “Just In Time Technology”
 - No technology before its time
 - Continuous cost reduction cycle

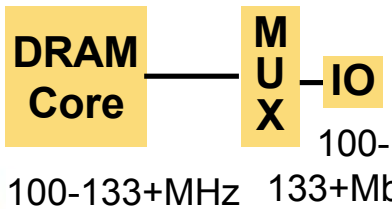
A Few Comments About Systems

- Systems must always be “good enough”
 - Must work in high volume production
 - But it is not necessary to over design
- Fundamental physics forces some limits
 - The DRAM core can only operate so fast
 - The trace routing in the system is becoming a significant part of the timing calculations
 - Signal integrity reflections can no longer be ignored

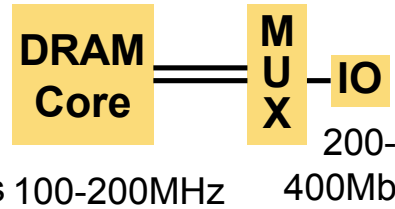
(S)DRAM Core & I/O Cycle Time,



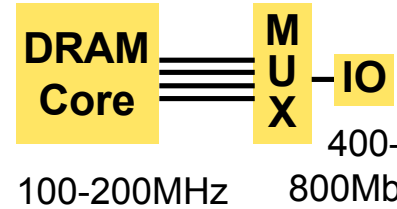
SDR: Prefetch of 1



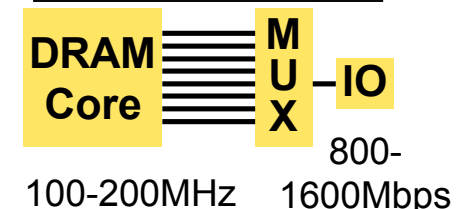
DDR: Prefetch of 2



DDR2: Prefetch of 4



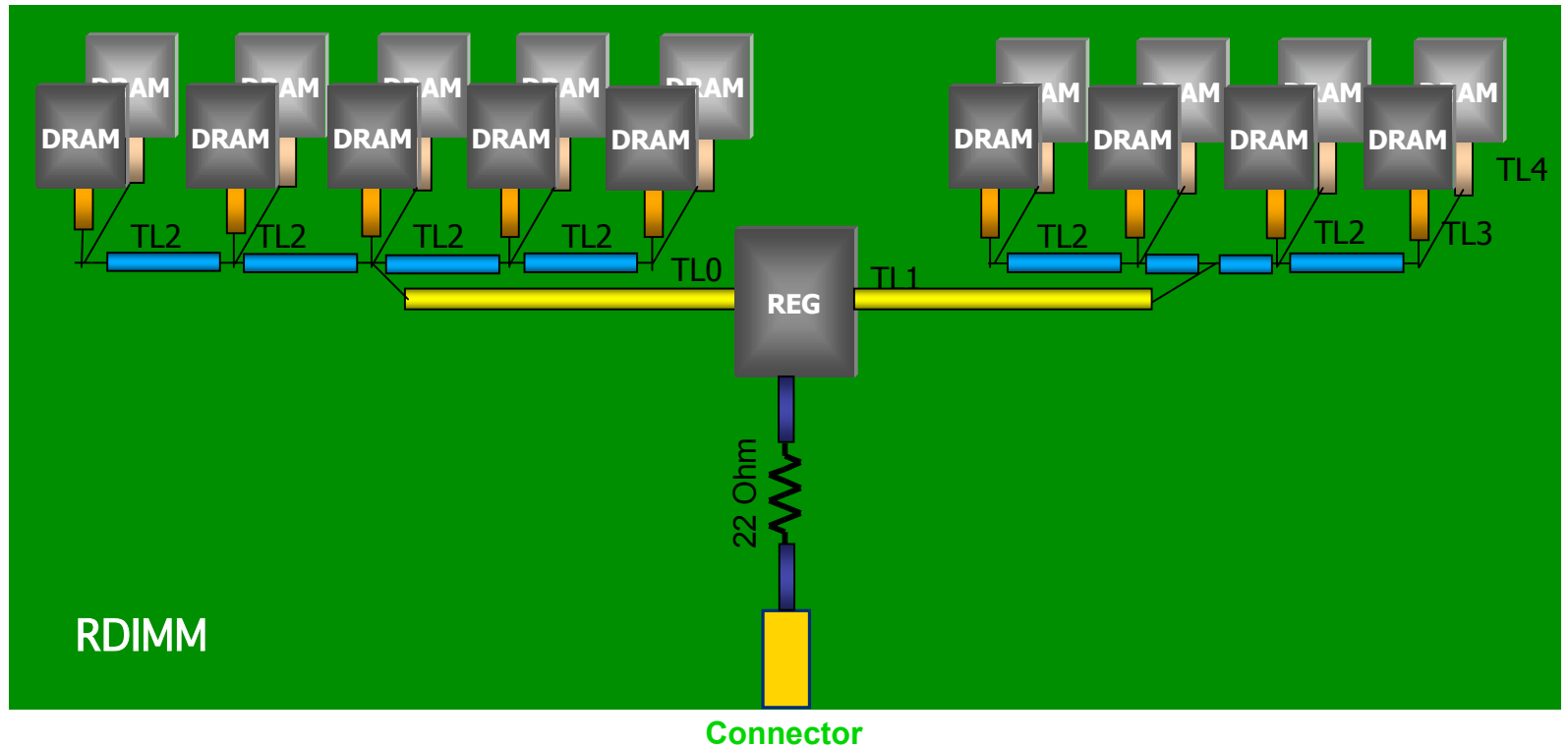
DDR3: Prefetch of 8



- DRAM core column cycle time is limited to about 5ns (200MHz).
- Prefetch defines minimum BL even if all bits are not used
 - The core column cycle time (tCCD) is required before any new cycle

Challenge: ADD/CMD Topology

Typical DDR/DDR2 ADD/CMD net for RDIMM/UDIMM:
“Un-terminated Hybrid T” (note: termination is on MoBo) - **Not good enough for high frequency**

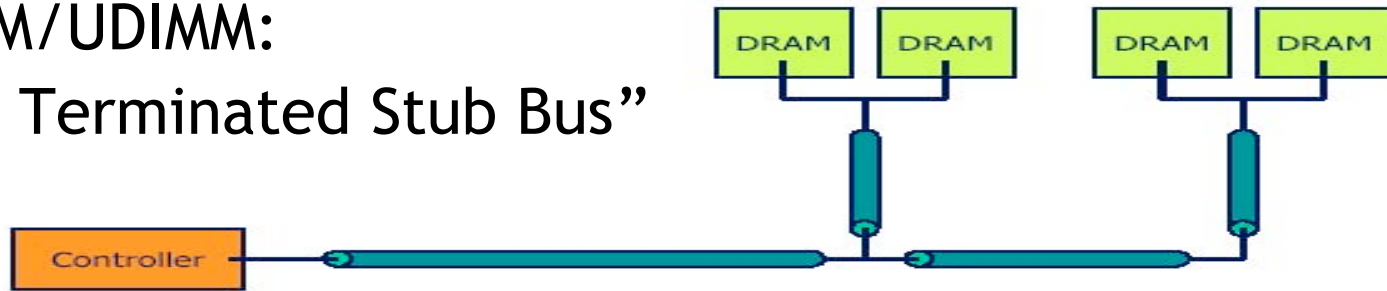


System Challenge: DQ Topology

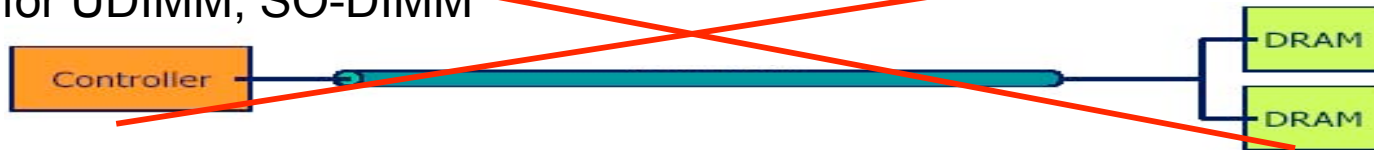
Typical DDR2 DQ net for
RDIMM/UDIMM:

“On-die Terminated Stub Bus”

New DDR3
Requirement



~~DDR3 Original Goal: Single slot system: P2P or P22P
for UDIMM, SO-DIMM~~

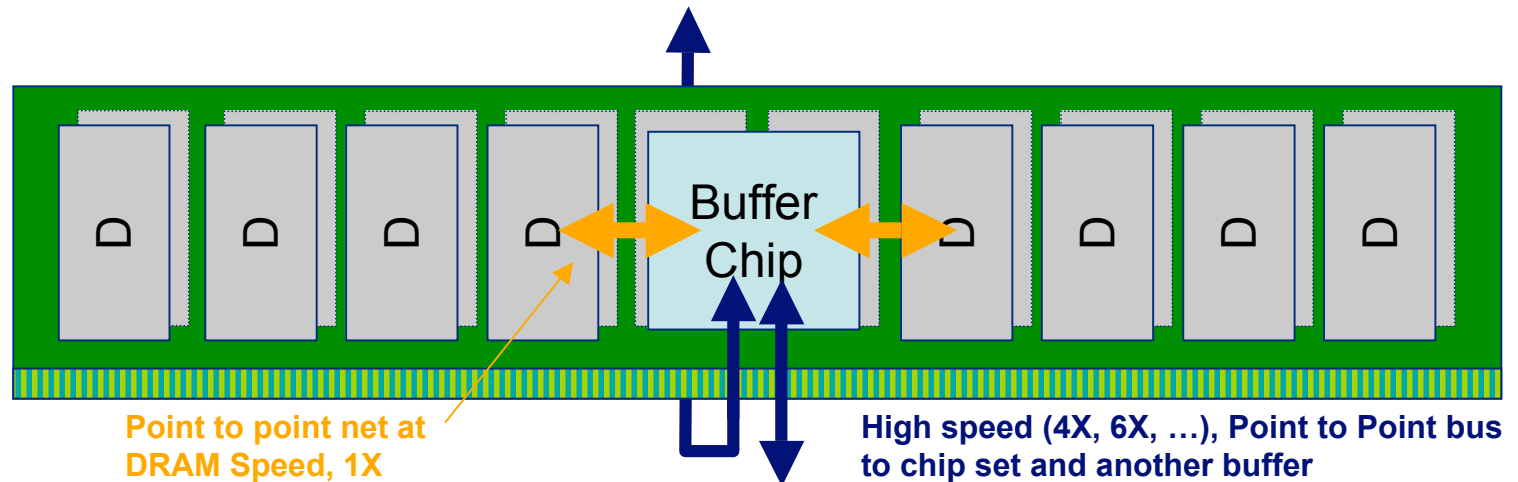


Discussions with end customers changed that Goal:
2 slot is a requirement for field upgrade on All DIMMs
so now DDR3 will follow the DDR2 - 2 slot basic system

Improved driver technology supports 2 slot up to DDR3 1600

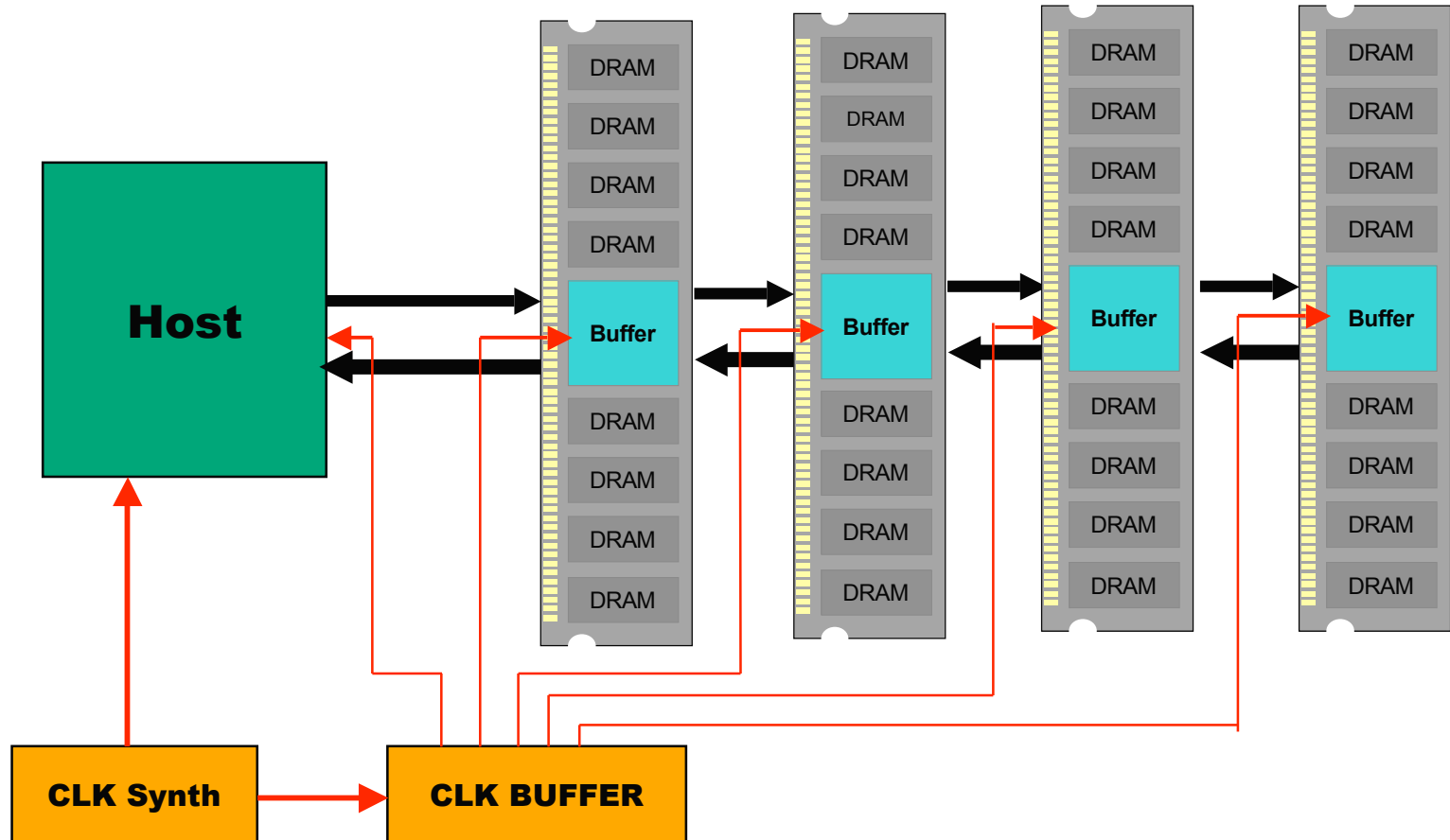
Buffer on DIMM (aka FB-DIMM)

Buffer on DIMM Proposed as a possible point to point net solution



- Address, Control and Data buffered
- High speed interface Controller to Buffer and Buffer to Buffer

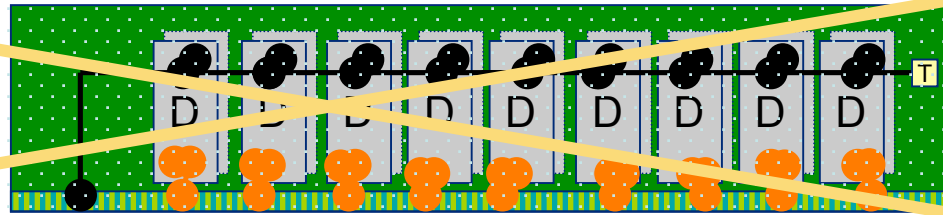
Possible Fully Buffered DIMM Structure



UDIMM DDR3 CMD/ADD Topology

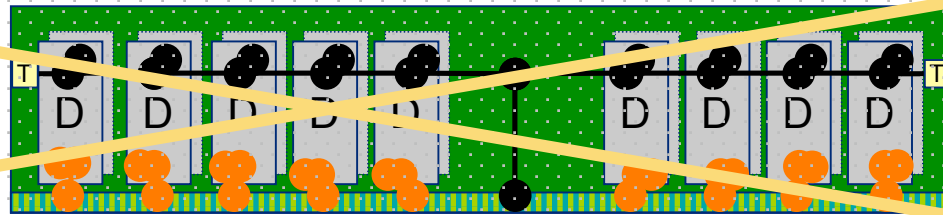
Option 1:

- 1 CA Copy
- left entrance
- 1N rule



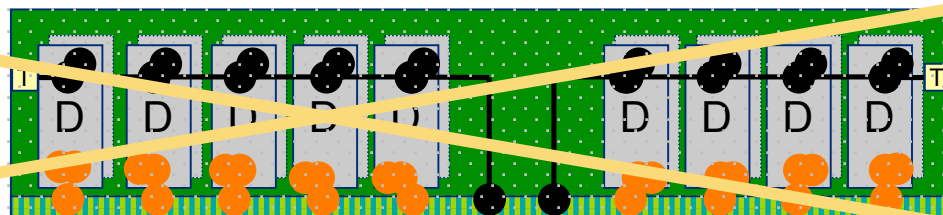
Option 2:

- 1 CA Copy
- center entrance
- 2N rule



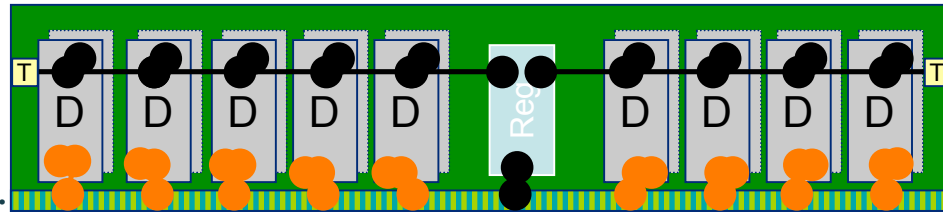
Option 3:

- 2 CA Copies
- center entrance
- 1N rule



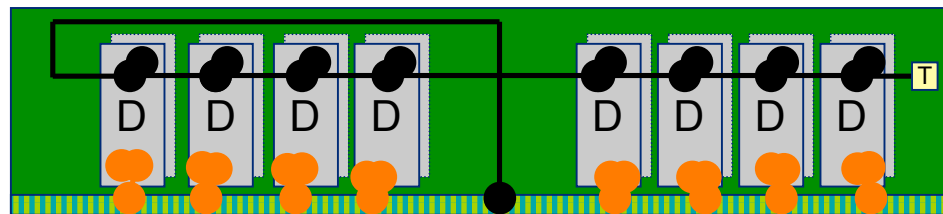
Option 4:

- 1 CA Copy
- center entrance
- 1N rule with Reg.



Option 5:

- 1 CA Copy (loop)
- center entrance
- 1N rule



CA, Clock
(fly by,
double drop)



DQ, DM, DQS
(P22P)

“DDR3
ADD/CMD/Control bus
has midlevel(VDD/2)
termination, which is
not supplied by the
DRAM”

“DDR3 SDRAM does
not supply termination
for the CK pins”

JEDEC Status - ADD/CMD Topology

- In all cases:

“Un-terminated Hybrid T”

Changes
to

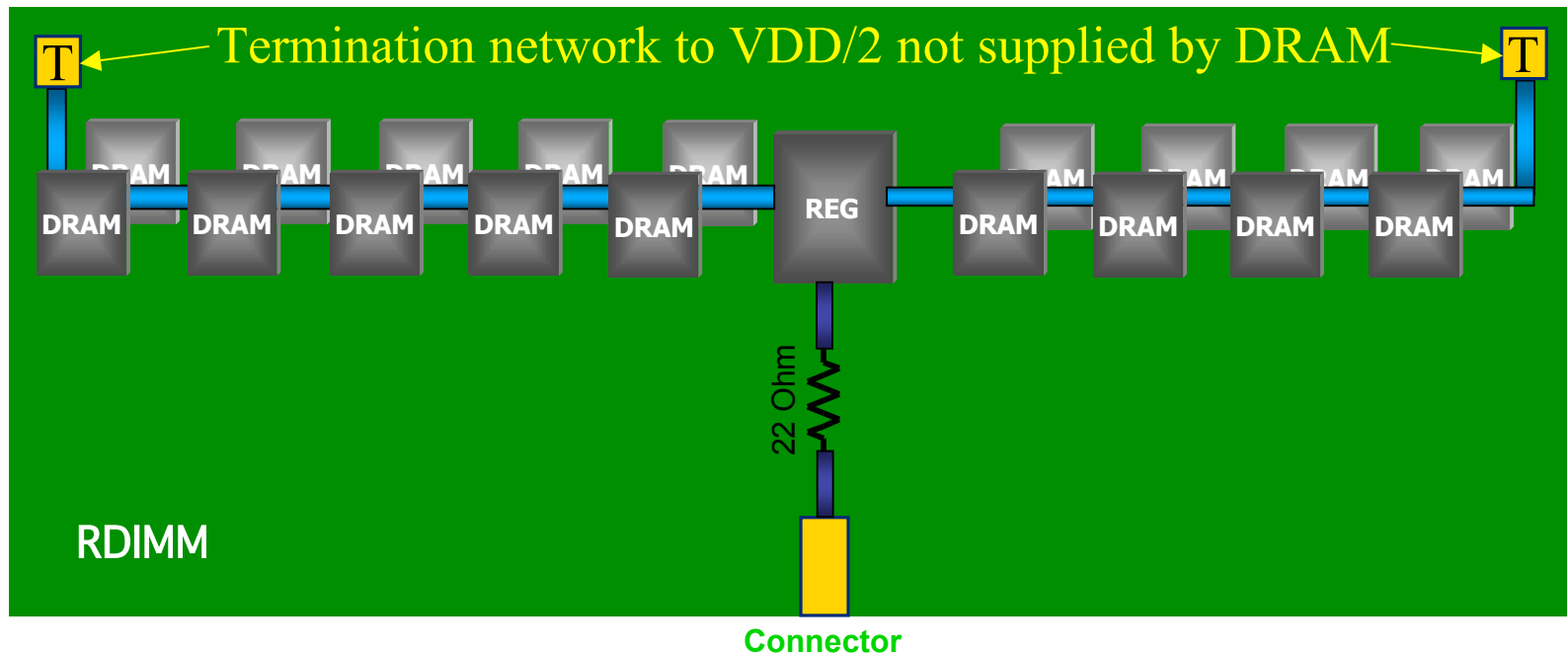
“End-terminated fly-by”

Terminated on-DIMM

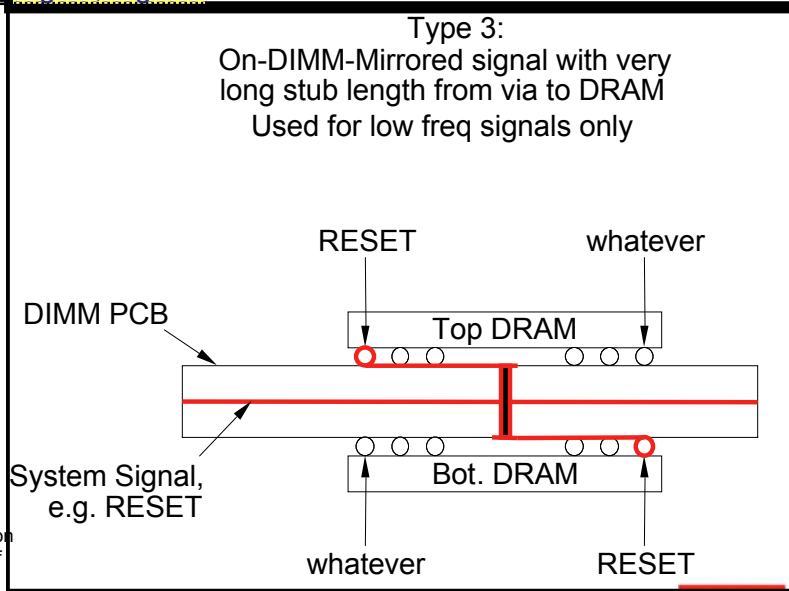
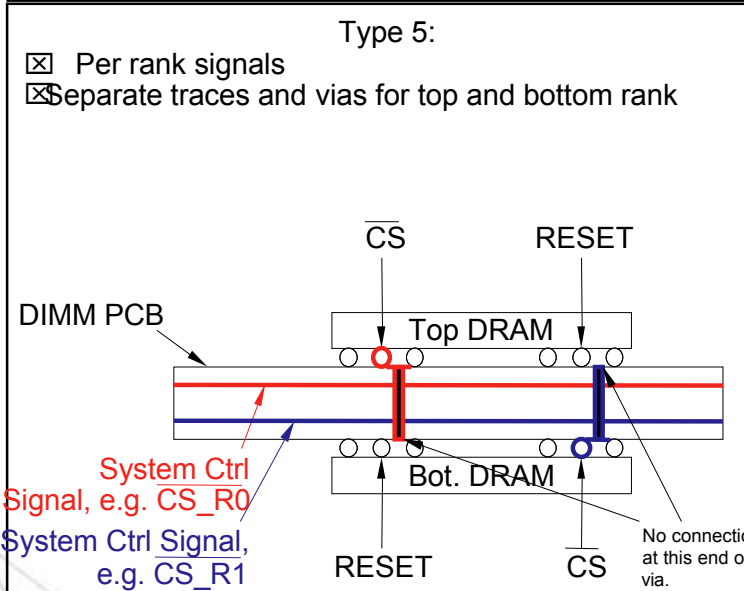
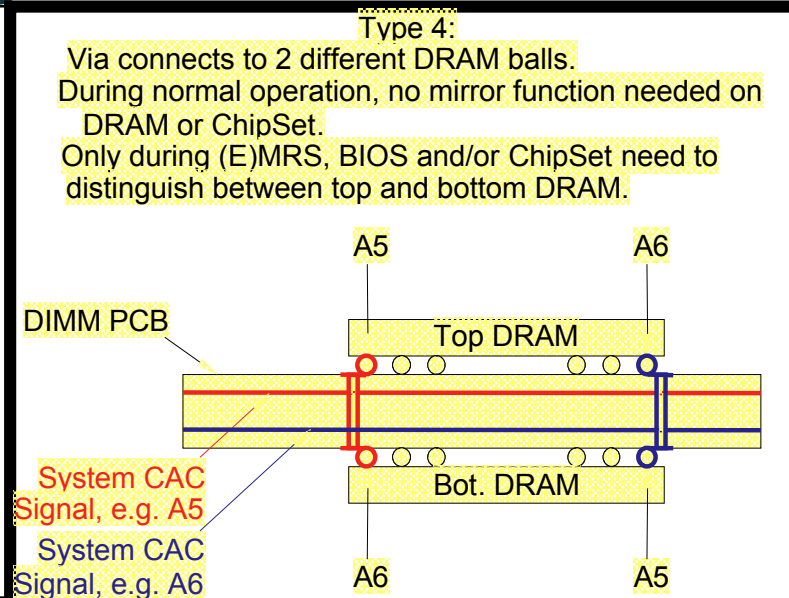
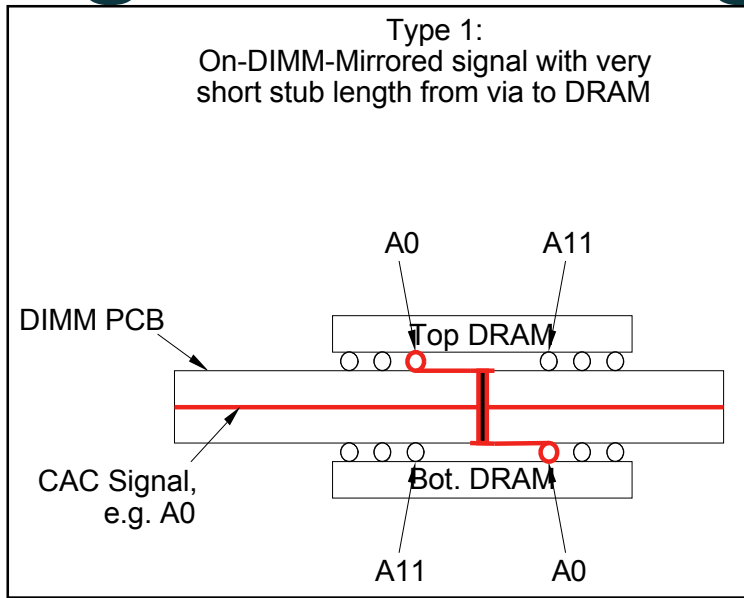
- Option 5, Center Entry with Loop,
decided for single slot UDIMM

Challenge: ADD/CMD Topology

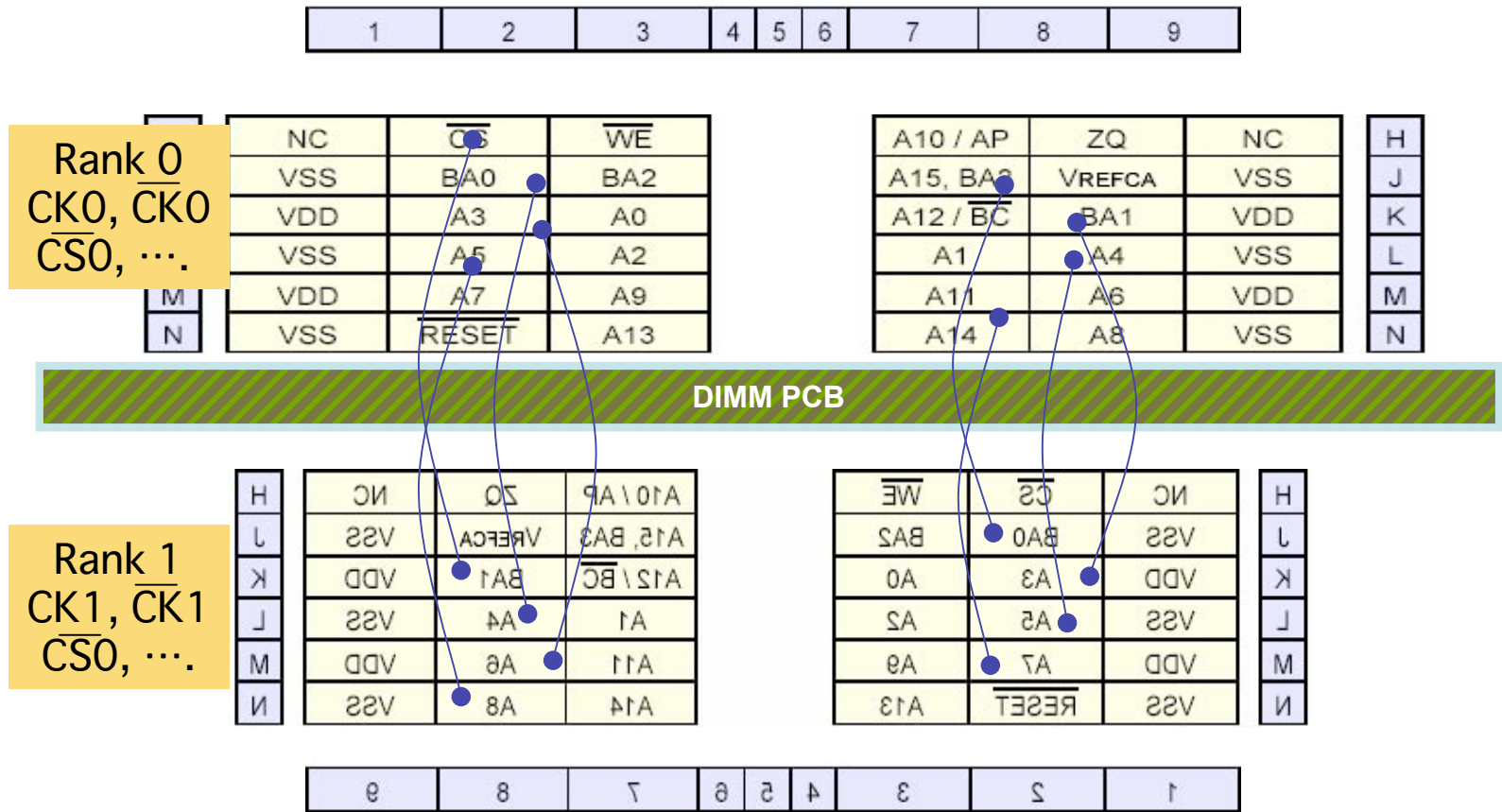
“End Terminated Fly-by” ADD/CMD net for RDIMM/UDIMM:
Acceptable for high frequency operation



Signal Mirroring for DDR3



Mirror Friendly DRAM Ballout



Mirrored Addresses: BA0, BA1, A3, A4, A5, A6, A7, A8

DRAM Finally Gets a RESET w/ DDR3

- DDR3 DRAM will implement a RESET function which is an asynchronous external control signal to DRAM.
- The RESET signal will force DRAM from operational or non-operational conditions into a defined state. After RESET, any previous data in the DRAM will be lost and the DRAM need to be re-initialized, including but not limited to loading mode registers and resetting the DLL
- The Reset can be asserted at any time, applied asynchronously to the DRAM during any cycle
- It is mandatory for system to hold RESET at active state at beginning of power ramp until power reaches a stable state
- The details on RESET procedures and functionality are still in discussion in JEDEC committees

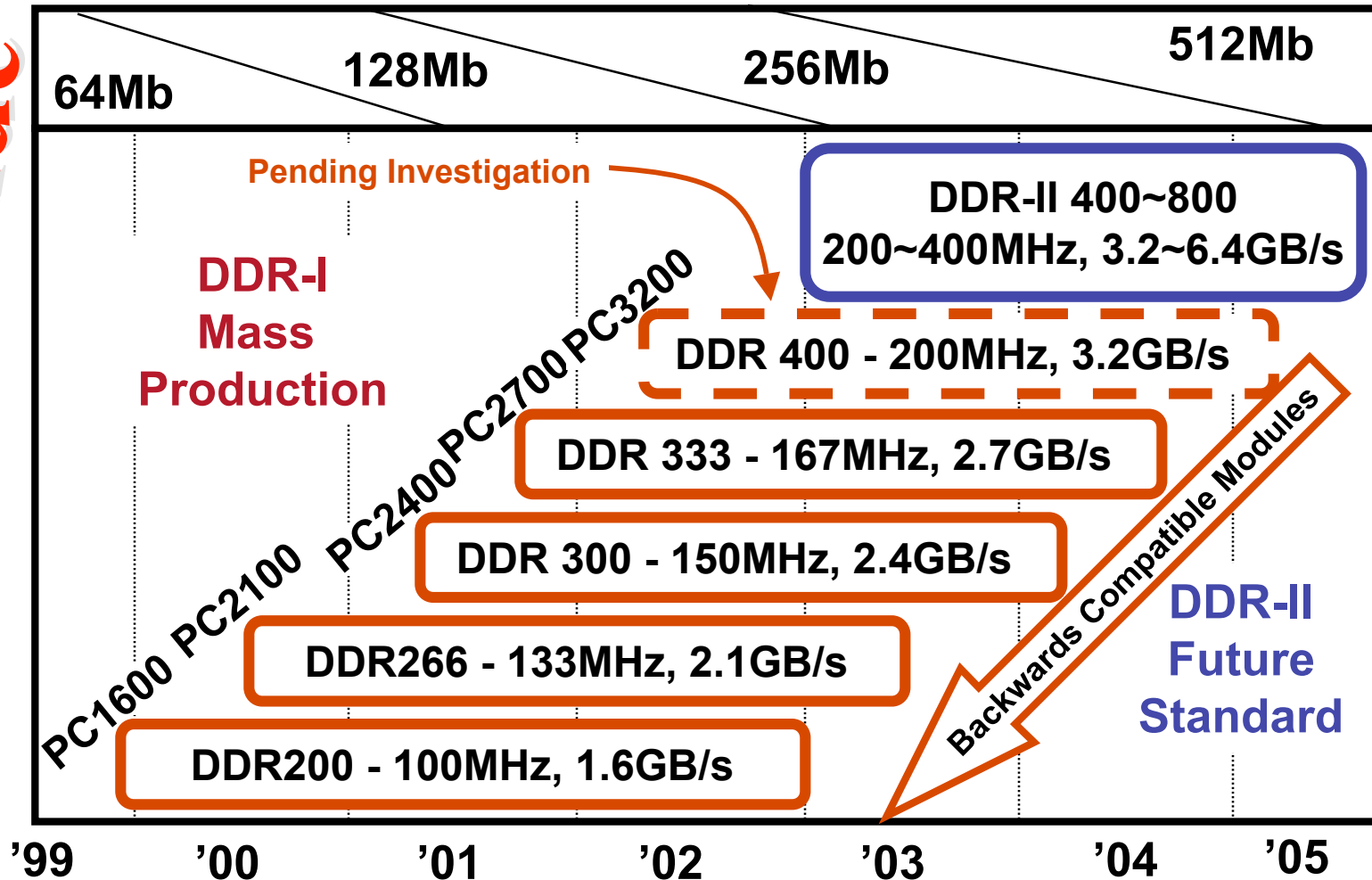
SDRAM Evolution (DDR3 preliminary)

	SDR SDRAM	DDR SDRAM	DDR2	DDR3
Data Rate [Mbps / pin]	PC66, PC100, PC133	DDR200, DDR266, DDR333,	DDR2-400, 533, DDR2-667, 800	DDR3- 800 to DDR3-1600(?)
Data Width	x4, x8, x16	x4, x8, x16	x4, x8, x16	x4, x8, x16
VDD = VDDQ	3.3 (+/- 0.3)	2.5 (+/- 0.2)	1.8 (+/- 0.1)	1.5 (+/-5%)
Interface	LVTTTL	SSTL_2	SSTL_18	?
# of banks	2 / 4	4	4 / 8	8/(?)
Prefetch	1 (2 & 8)	2	4	8*
Burst Length	1, 2, 4, 8, (page)	2, 4, 8	4, 8	8 & Burst Chop 4*
Strobe	No	Single	Single/Differential	Differential
tAC / [ns]	3.0 (tOH) ... 5.4	+/- 0.75 (DLL)	DDR-like	DDR-like
DQ drive strength	Wide envelope	Narrow envelope	OCD Calibration	OCD w/ ZQ Cal *
Termination	None	MoBo	Mobo/ODT	ODT with ZQ Cal *
Read Latency	CL=(1),2,3	CL=(1.5),2,2.5,(3)	CL=(2),3,4,5	CL=5-10,(11)
Additive Latency	No	No	AL=0,1,2,3,4	AL=0,CL-1,CL-2
Write Latency	0	1	RL - 1	5,6,7,8
Data Mask	Yes	Yes	Yes	Yes
Interrupts	Yes	Yes	W-W, R-R 4n only	No, BC4 on the fly*
DRAM Reset	No	No	No	Yes *
Package	TSOP-54	TSOP-66 / BGA	BGA	BGA w/ Mirroring *

DDR Performance Migration Path

The "Mainstream" memory module migration path *(Presented in 2000)*

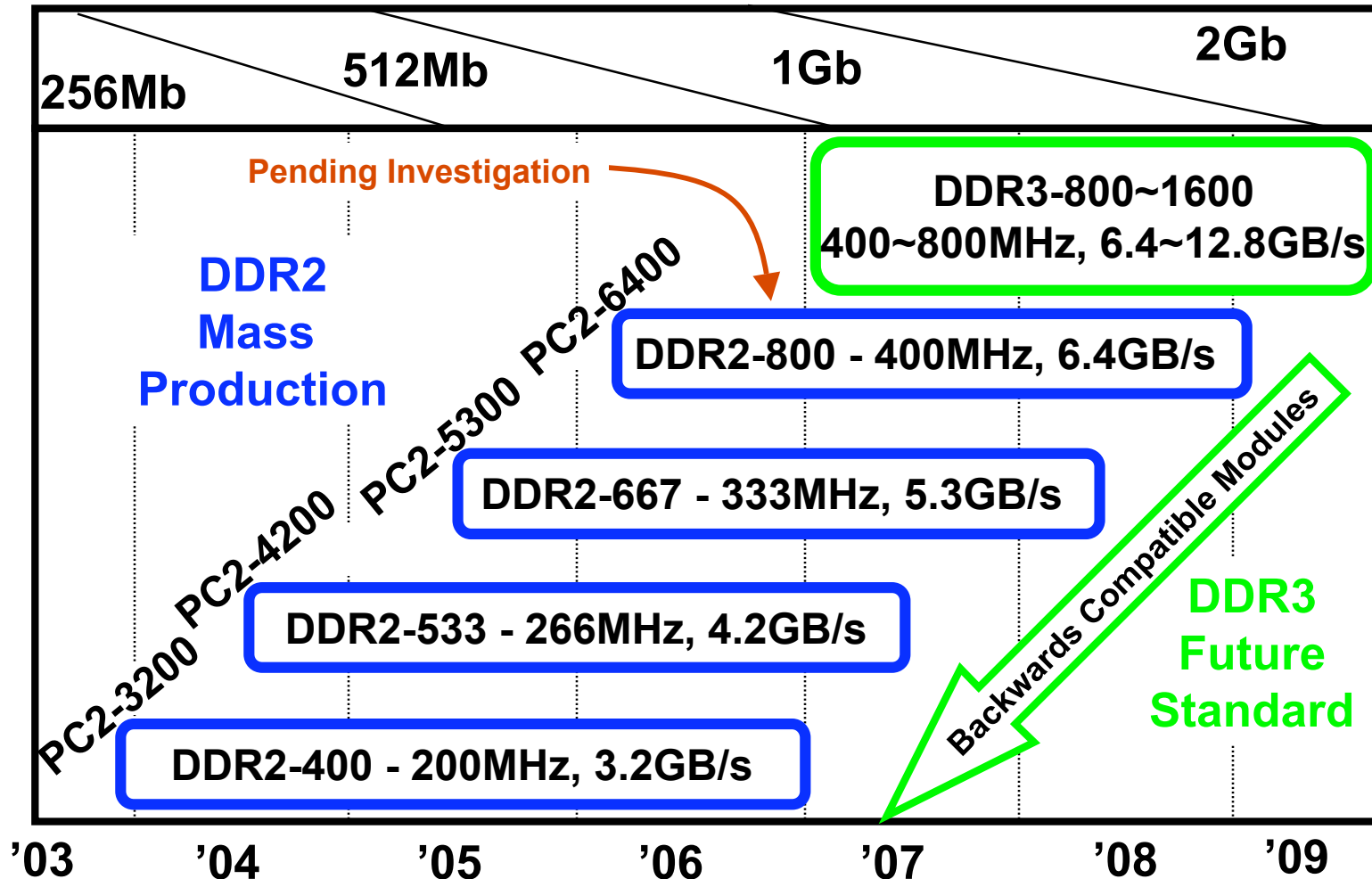
History Slide



Watching the past predicts the future

DDR2 Performance Migration

The "Mainstream" memory module migration path



Amazing similarities to the past

Conclusions

- Even though new DRAM generations come most things stay the same for successful DRAM
 - If you want to know the future look at the past
- DDR2 is for designs now with speeds from 400-800Mbps/pin
- DDR3 is under development for speeds from 800-1600Mbps/pin (it is not finished yet!!!)
- Customers ultimately have more power than anyone else in the DRAM business

Thank You

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