

VTF 2006

VIA Technology Forum

SOI Technology Benefits for UMPC Processors

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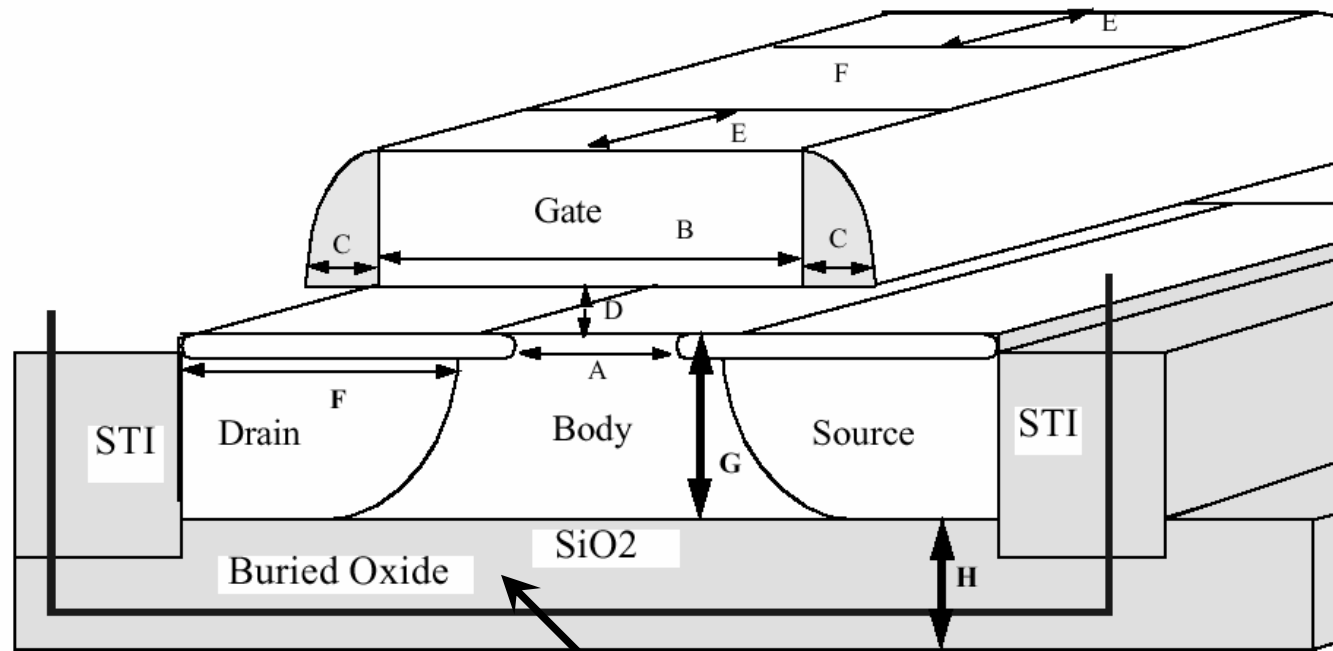


*Embracing
Digital Intelligence*

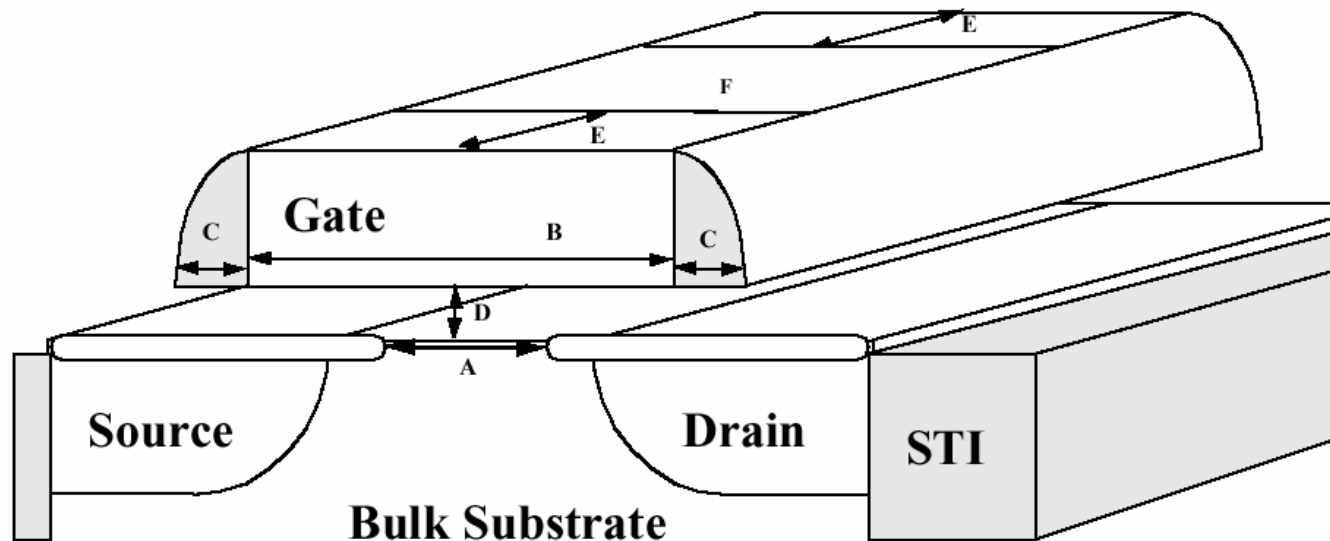
Outline

- **SOI Technology Introduction**
 - What is SOI - Silicon On Insulator
- **IBM 90nm SOI Technology**
 - SOI + Copper Wiring with low k dielectric
 - Strain for higher transistor performance
- **Benefits of SOI**
 - Performance
 - Power
 - Leakage
- **Application to UMPC**

SOI Device



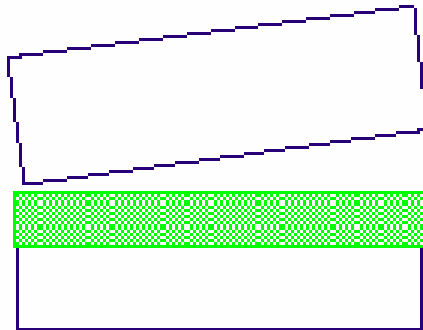
Bulk MOSFET Device



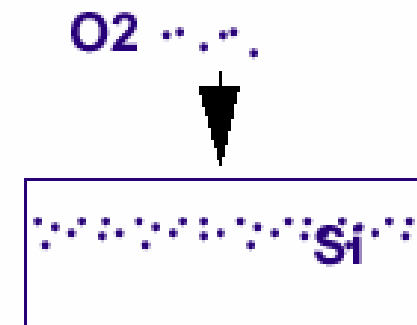
**Buried Oxide
Under Transistors**

Commercial SOI Substrate Processes

- Bond Oxide and Si

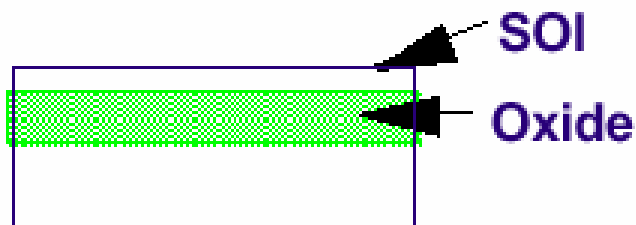


- Implant Si with Oxygen:

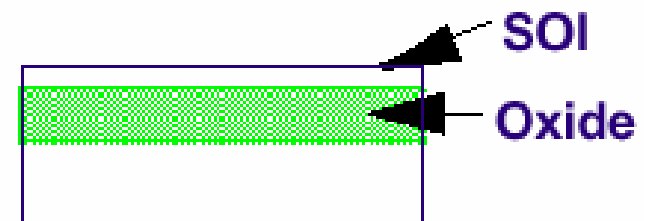


or

- Etch back



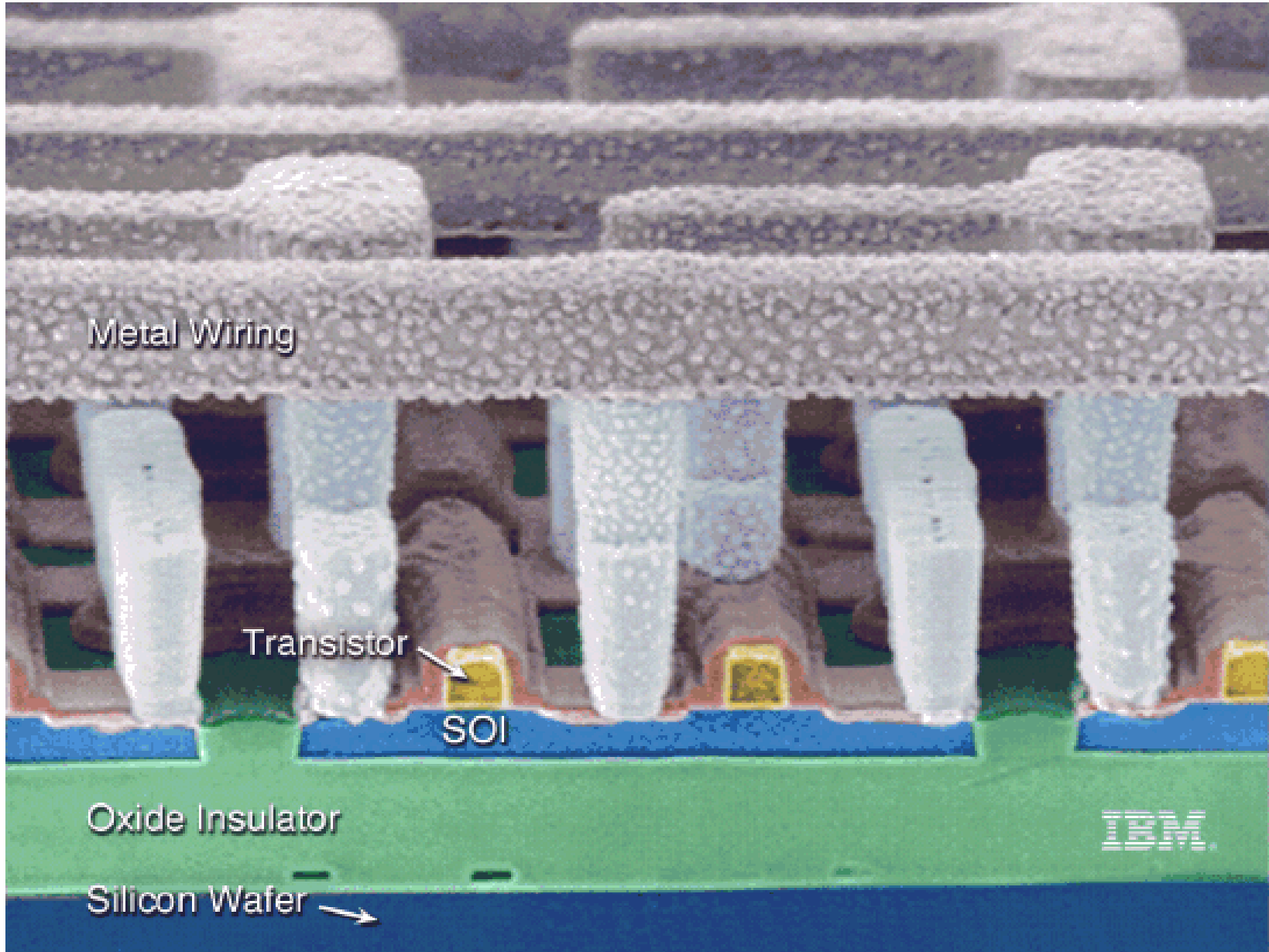
- Anneal damage:



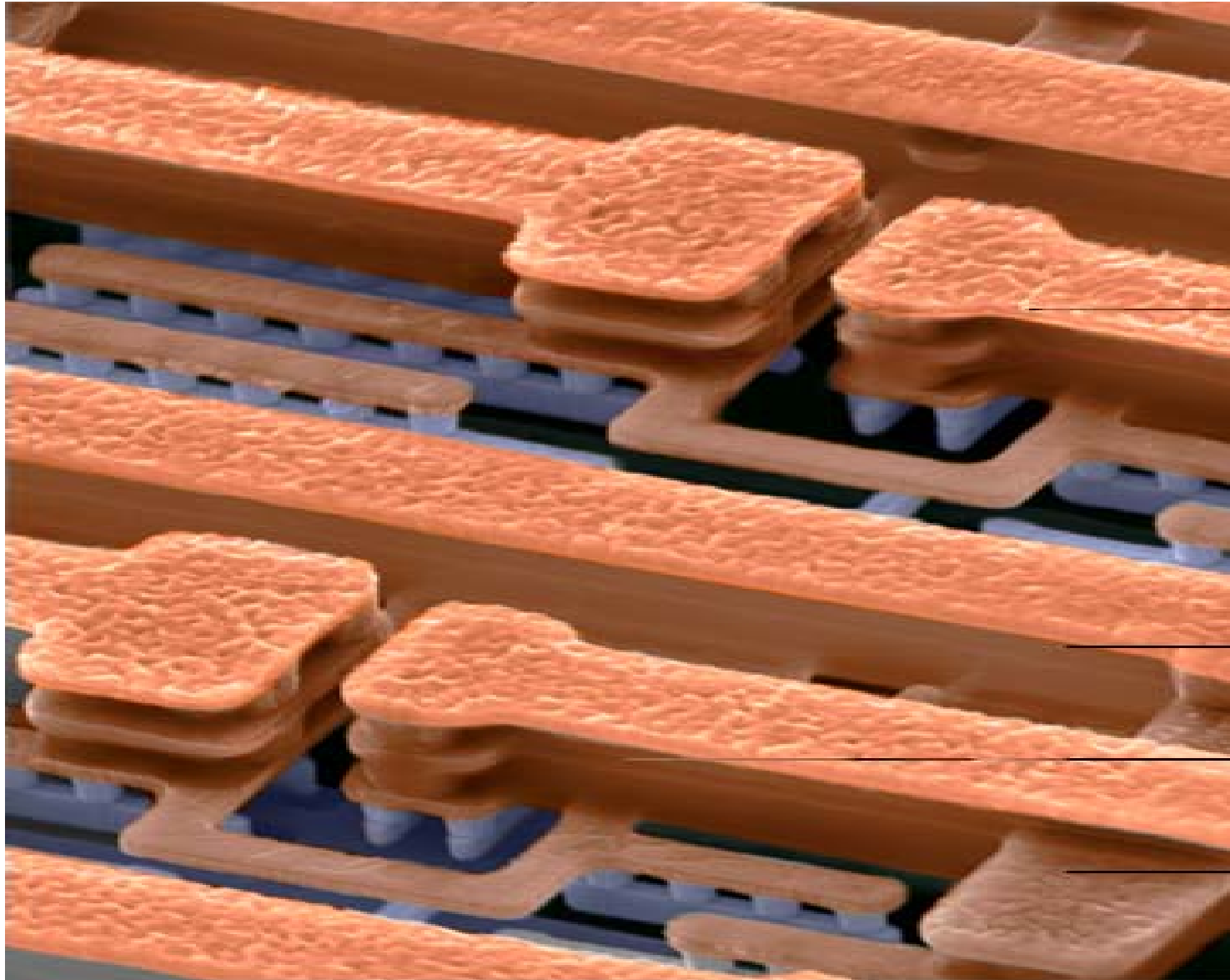
SOI Technology Advantages

- **Higher Performance / Lower Power**
 - Capacitance Reduction
 - Oxide below transistor reduces junction capacitance
 - Shorter transistor gate length
 - Better control of threshold voltage
 - Lower device threshold
 - Improved low voltage operation
- **Improved isolation / better density**
 - No latchup
- **Lower Leakage at High Temperatures**
- **Reduced Soft Error Rate**

SOI in Production 180nm, 130nm , and 90nm



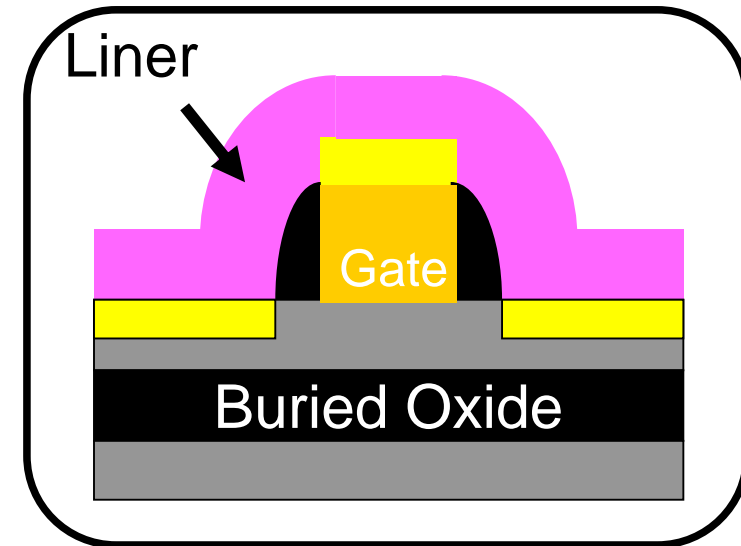
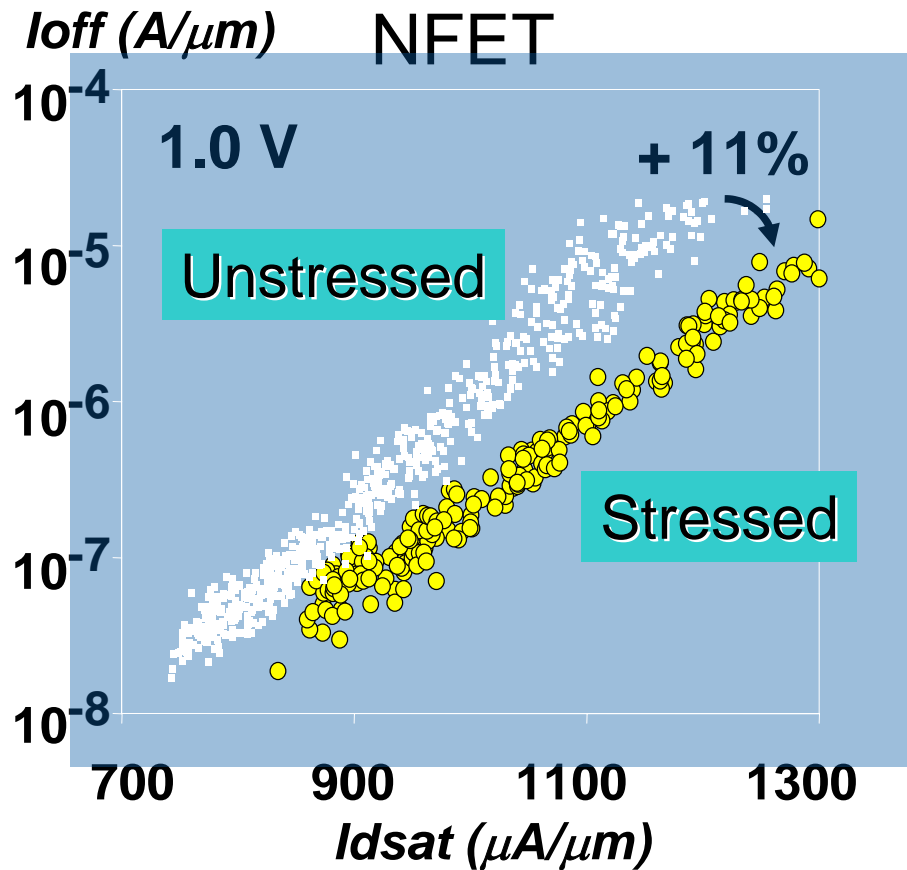
Copper Wiring



IBM SOI 90nm Technology

- **Technology Features**
 - 46 nm Channel Length
 - Local strain for n-fet performance boost
 - 1.0V Operation (nominal)
 - Dual Gate Oxide Process
 - 11.2A Tox for high performance transistors
 - 22A for high voltage transistors
 - Local Interconnect
 - 10 levels copper wiring with low dielectric constant insulator (low k)

IBM SOI 90nm Technology

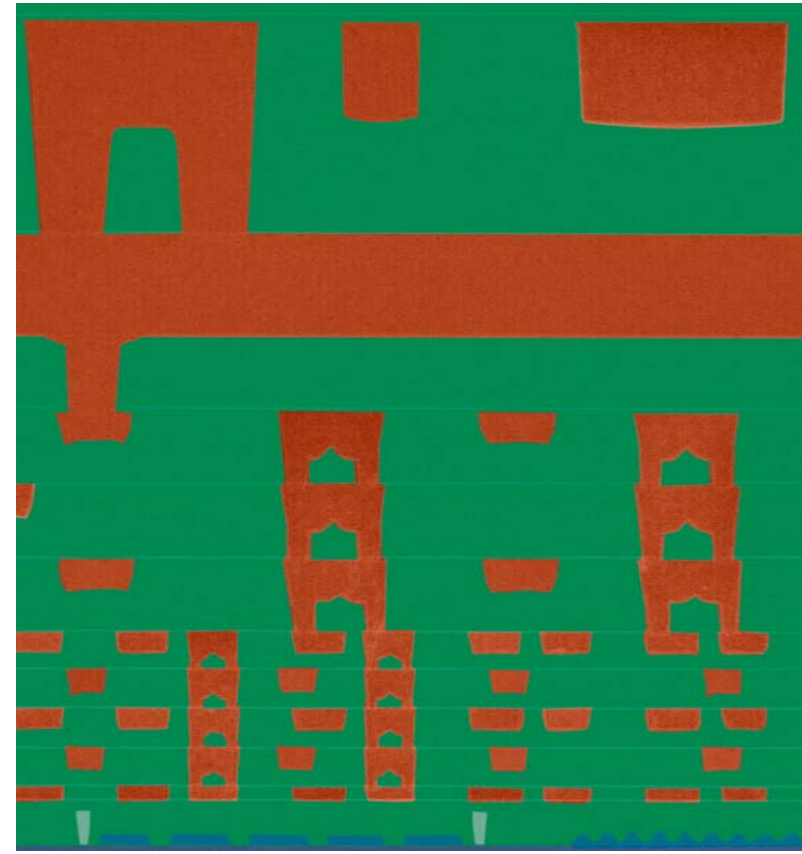
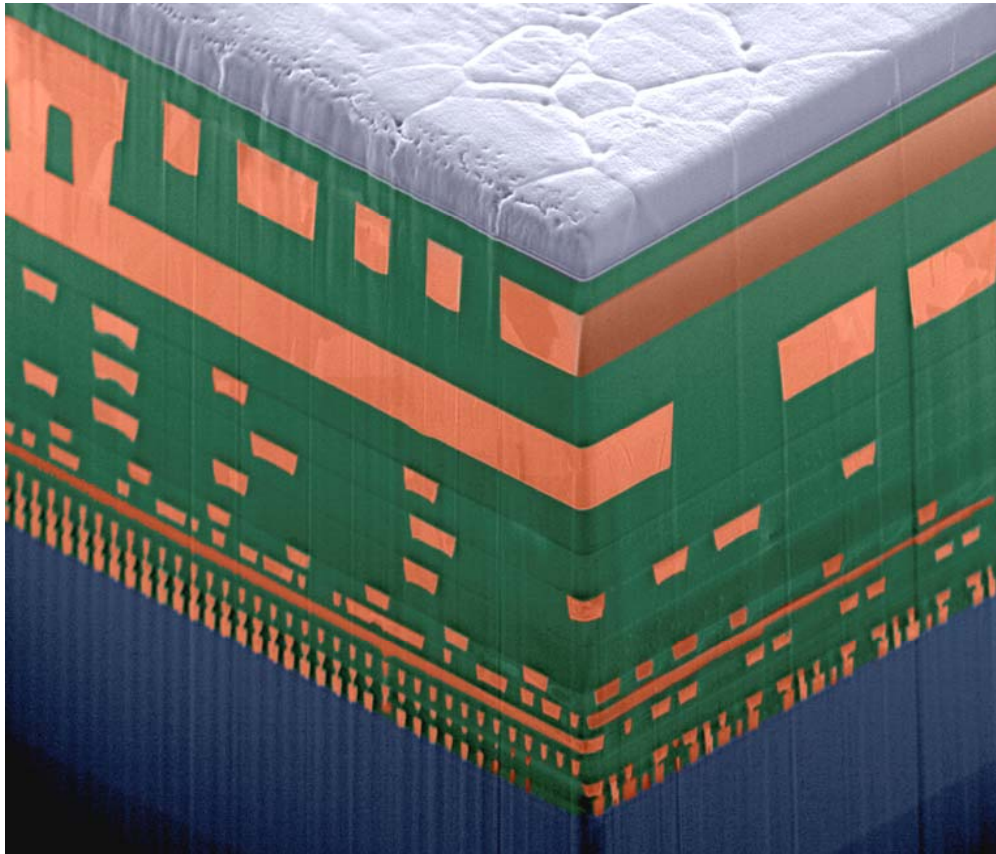


Stress Liner enhancement

Tensile Liner boosts Nfet

Effective Drive Current ➔ **NFET : +15%**

90nm Microprocessor Cross-Sections



M10, 6x

M9, 6x

M8, 2x

M7, 2x

M6, 2x

M5, 1x

M4, 1x

M3, 1x

M2, 1x

M1, 1x

M0, (W)

Metal levels:

W: 1 local interconnect level plus contact level

Cu: 10 levels - first 8 levels in low-k, final 2 in SiOF

Al: 1 terminal metal level, used for pads and wiring

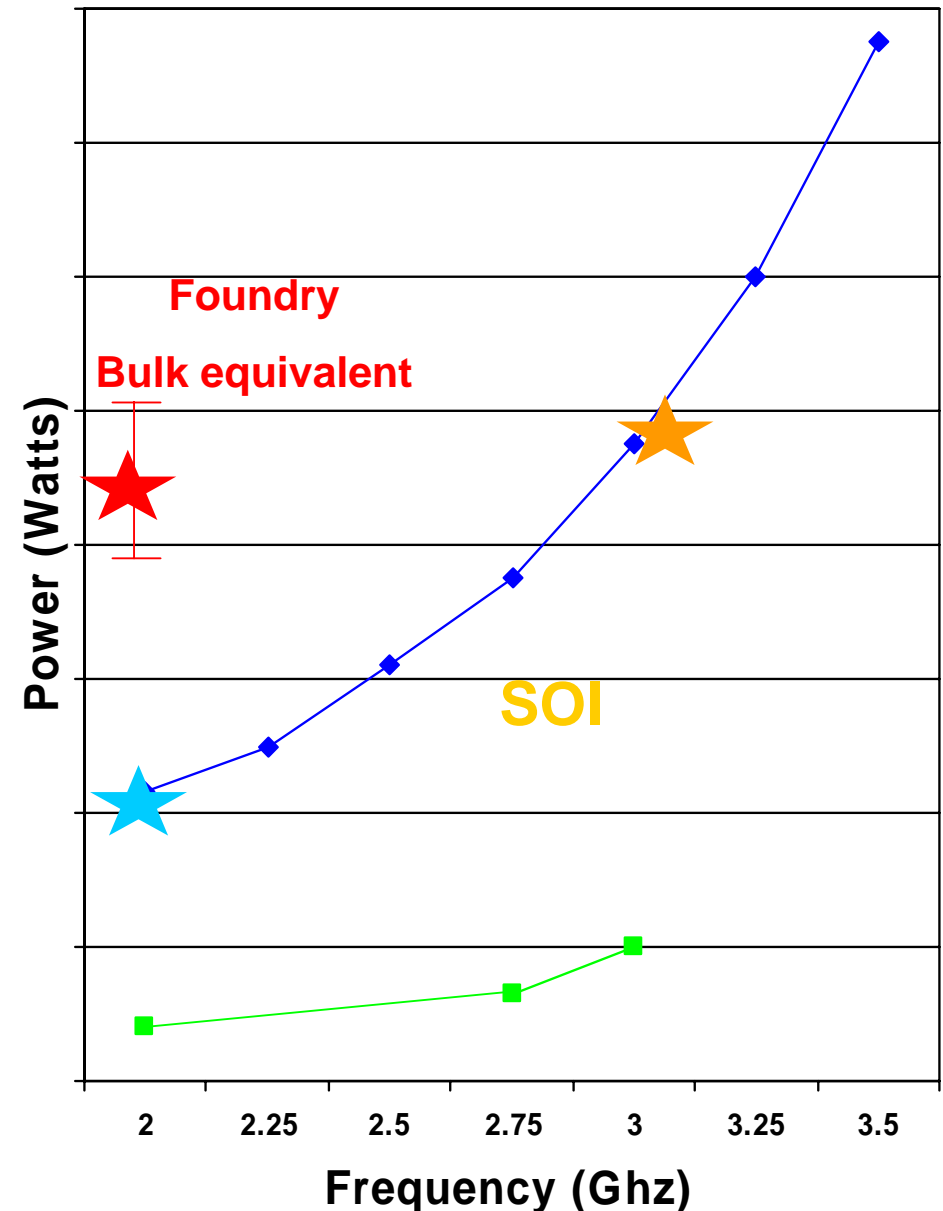
SOI Performance Advantage

- **IBM SOI ~ 20% - 30% faster than industry standard foundry bulk technology**
- **IBM experience**
 - 10% performance can be traded for 30% reduction in total power

IBM 90nm Processor Experience

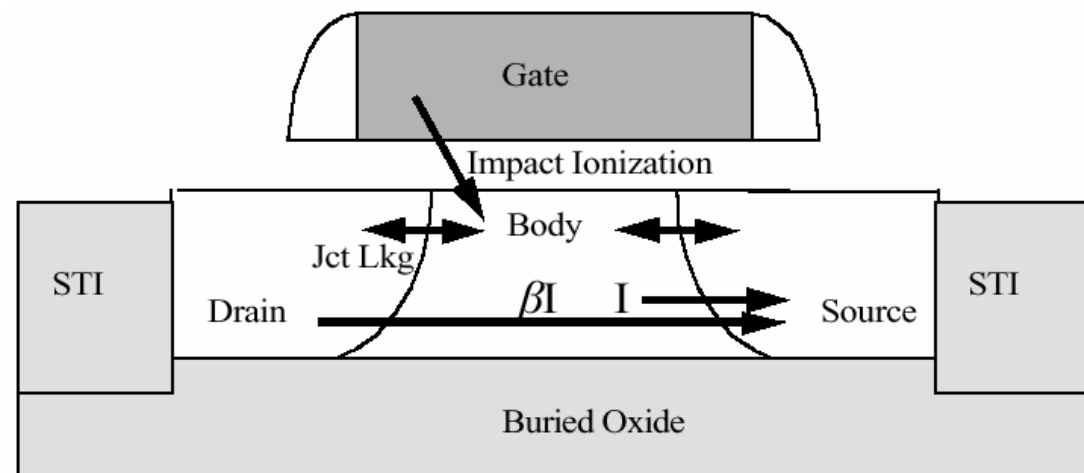
Active Power Capability of SOI

- Dropping Vdd to lower performance 10% reduces power by ~30%
- Simulations of design in bulk shows much higher power and poorer performance

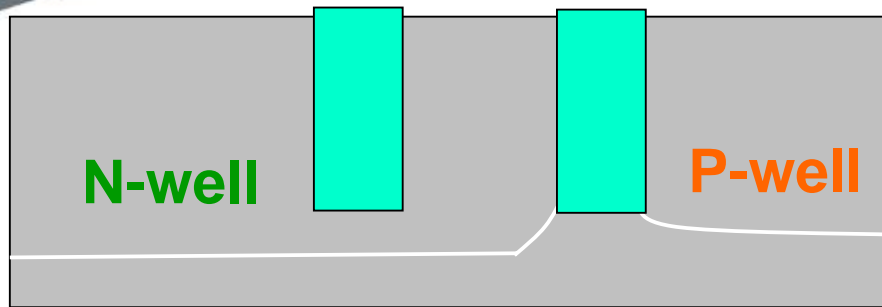


Leakage Advantage of SOI

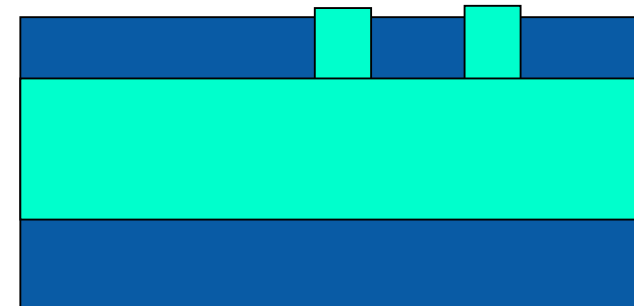
- **MOSFET Transistor leakage increases at high temperature**
 - **V_t (threshold voltage) drops ~ 0.8mV/C**
- **SOI Transistor leakage increase at high temperature smaller**
 - **floating body + drain junction leakage raises V_t to compensate for natural V_t drop**



SOI Cost Advantage



Bulk



SOI

Substrate cost

+ higher

In Fab Wafer Processing
(Simpler isolation, implants)

- lower

Good Chips / Wafer (density, CLY)
(smaller chips, simpler process)

- lower

Cooling Costs (lower power)
Power Costs (regulated power supplies)

Lower
Lower

Total Packaged Die Cost Advantage

Lower

VIA C7 - Designed for Mobility

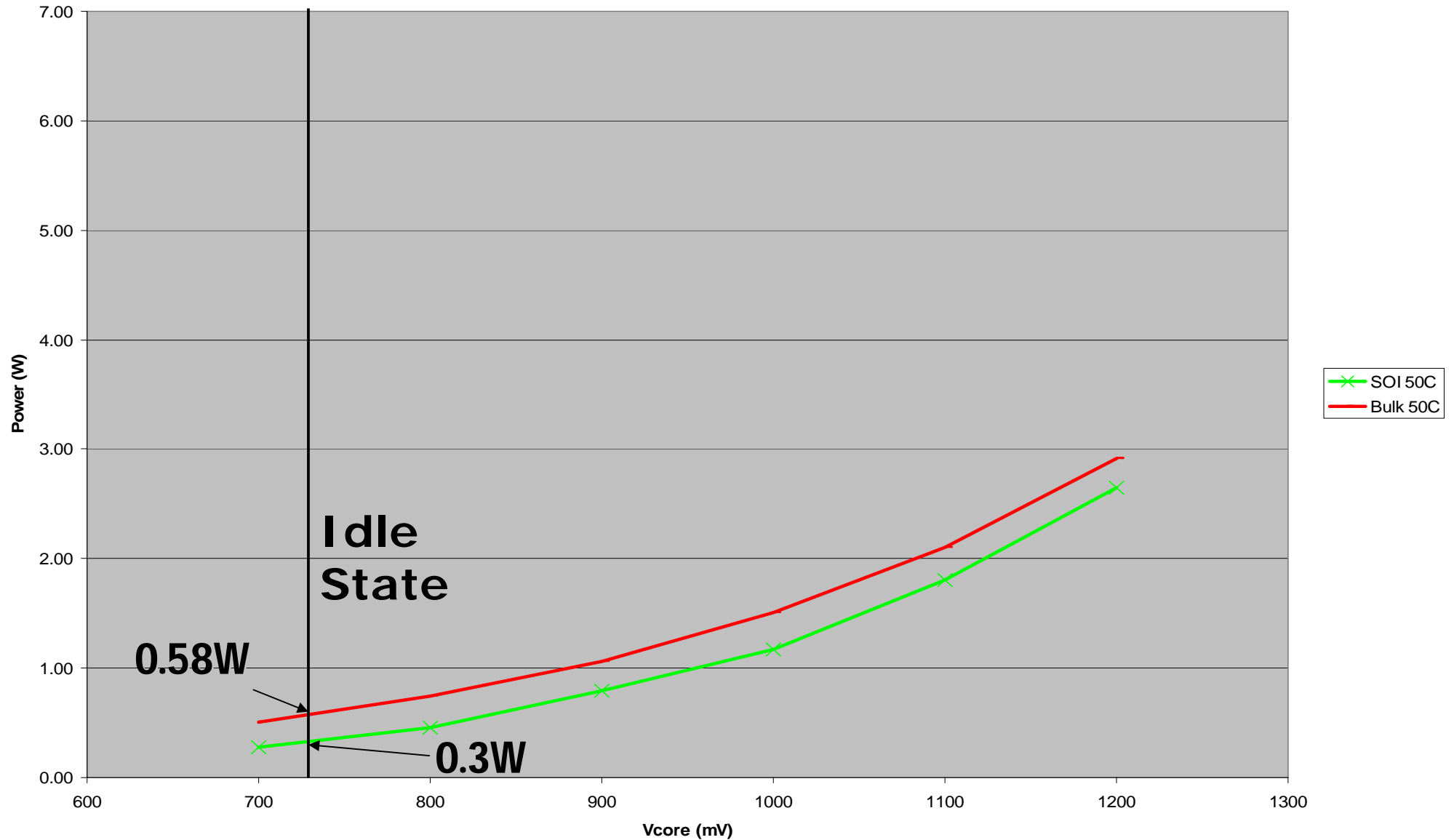
- **Extends VIA leadership in reducing *MAXIMUM* power**
 - Lower Thermal Design Point (TDP) to reduce the size and weight of cooling system
- **Adds new features to reduce *AVERAGE* power**
 - Rapidly accomplish computing tasks and then reduce power to minimize battery drain
- **Increases performance on mobile applications**
 - New features and speeds up to 2 GHz

VIA C7-M Details

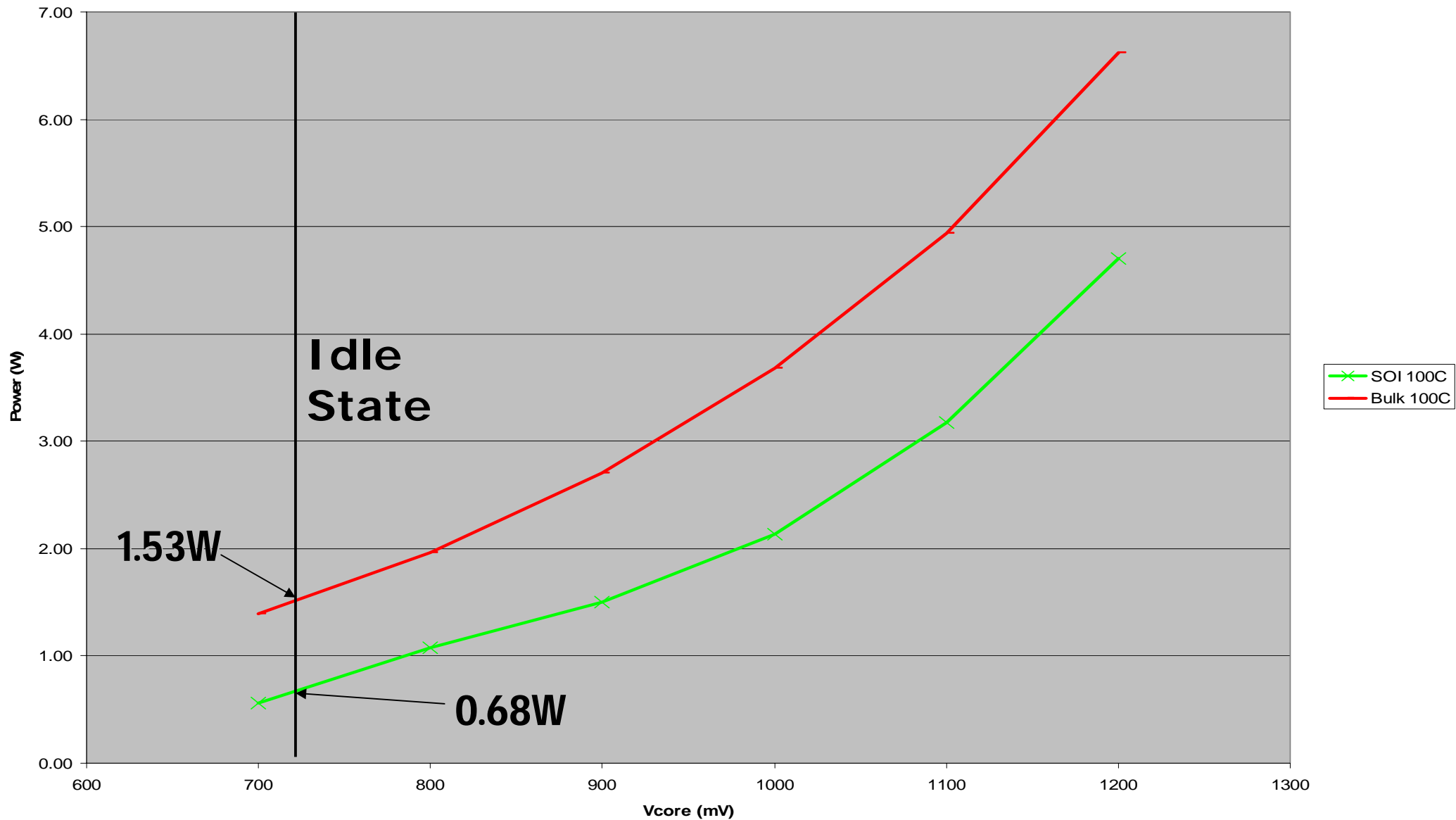
- **World class IBM Foundry using 90 nm SOI**
- **TDP-2.0 GHz @ ~20W and 1.0 GHz ULV @ 3.5W**
 - Windows Idle is 0.25W
- **nanoBGA2**
 - Ultra small BGA 21mm x 21mm for lightest & thinnest notebooks
- **With More Functionality:**
 - SSE3
 - Up to 800 MHz FSB (1066 MHz possible)
 - Enhanced PowerSaver
 - Power reduction technology using dynamic frequency and voltage adjustments
 - TwinTurbo PLL's
 - C7-M has two core clock PLL's for fastest frequency transitions
 - Snooping can occur during transitions
 - Security features
 - AES, RNG, SHA-1/256, & RSA modexp primitive
 - NX bit for memory protection.
 - Dual and Quad processing

- **C7-M Performance in SOI**
- **Reduction in Vdd allows large Power saving**
 - TDP-2.0 GHz @ ~20W and 1.0 GHz ULV @ 3.5W
- **Design built in IBM 90nm SOI and compared to same design in high performance bulk technology**
 - Windows Idle is 0.25W in SOI
 - At 50C bulk idle power is ~1.8x SOI
 - 0.3W vs. 0.58W
 - At 100C bulk idle power is ~2.25x SOI
 - 0.68W vs. 1.53W

ACPI C4 Power @ 50C 90nm SOI vs 90nm Bulk



ACPI C4 Power @ 100C 90nm SOI vs 90nm Bulk



Summary

- **SOI Technology in production at IBM since 180nm generation**
- **90nm SOI contains additional performance elements**
 - SOI + Copper Wiring with low k dielectric
 - Strain for higher transistor performance
- **World class performance translates to world class low power**
 - Reduction in Vdd to minimize active power
 - Leakage / Idle power at high temperatures inherently better than bulk technology
- **Application to UMPC verifies benefits**